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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/079,336	02/19/2002	Vladislav Vashchenko	P05143	7946

7590

03/02/2004

Jurgen K. Vollrath  
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San Jose, CA 95125

EXAMINER

BENENSON, BORIS

ART UNIT PAPER NUMBER

2836

DATE MAILED: 03/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/079,336

Applicant(s)

VASHCHENKO ET AL.

Examiner

Boris Benenson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 02/19/2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) 1-10 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 11-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

*Election/Restrictions*

DETAILED ACTION

*Election/Restrictions*

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claim 1-10, drawn to semiconductor structure, classified in class 257.

II. Claims 11-19, drawn to ESD protection circuit, classified in class 361, subclass 113.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because ESD circuitry does not require specifics of claimed diode. The subcombination has separate utility such as a diode structure

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that provides more than one current path between an anode and a cathode and can be used in different applications.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Jurgen Vollrath (49098) on 1/23/2004 a provisional election was made without traverse to prosecute the invention of an ESD protection circuitry and an ESD protection method, claims 11-19. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-10 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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5. Claim 11-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art in view of Kim (5,859,758) and Lee (5,565,790). Applicants describe in Background of the Invention section of the Specification typical circuit wherein low resistive power supply rails (VDD, VSS) are provided and pad (Fig.1, Pos.10) connected by means of p-well diode (12) to VDD bus and by means of n-well diode (14) to VSS bus. A protected circuit (16) is protected by an ESD clamp (18) connected between VDD and VSS. Prior Art does not teach using a semiconductor structure wherein a first anode/cathode contact is an input to the structure and a second contact to a region of the same polarity as the first contact is an output from the structure and the first contact is separated from the second contact by a well region to provide a voltage drop between the contacts under ESD current pulse conditions that reducing the voltage to which a protected circuit is exposed.

Kim (5,859,758) teaches an Electro Static Discharge Protection Circuit, that include a primary ESD protection (Fig.3a, Pos. 31-32) and a secondary ESD protection (33-36), wherein a first anode/cathode contact (Node A) is an input to the structure and a second contact to a region of the same polarity as the first contact (Point between anode of diode 33 and cathode of diode 35) is an output from the structure. The

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primary ESD protection is providing a primary path for ESD current, if voltage become higher or equal to  $V_{dd} + V_{on}$  or lower or equal  $V_{ss} - V_{on}$ . The secondary ESD protection is providing a secondary path for ESD current, if voltage become higher or equal to  $V_{dd} + V_{on}$  or lower or equal  $V_{ss} - V_{on}$ . If applied static electricity is excessive, the current flowing through the primary path is increased. Thus, the potential of the node A becomes higher and a leakage proportional to the potential at the node A flows through the secondary path. It protects diodes of the primary path from being destroyed by excessive static electricity. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Applicant's Admitted Prior Art with teachings of Kim and include a secondary path, because it protects diodes of the primary path from being destroyed by excessive static electricity.

Lee (5,565,790) teaches an ESD protection circuit, wherein resistor (Fig.1, Pos.28) is installed between a primary device (15) and a secondary device (20). That resistor provides a voltage drop between an input pad and protected circuitry and limits a current flowing through protected circuitry. "The drain diffusion (17) of the field transistor (where the pad is connected and where an ESD voltage appears initially) and the drain diffusion (19) of the triggering transistor are spaced

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apart and the intervening region of the n-well forms a resistor (28)" (Col. 3, Lines 18-22). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify previously modified Prior Art and install a resistor between anodes/cathodes of the primary and the secondary protection circuits, because it will protect internal circuitry from exposure to maximum voltage of ESD spike even before the secondary circuit diverts such spike to a power rail.

Referring to Claims 15 and 17, each bipolar junction transistor of a structure on Figure 11 is connected as two diodes, wherein a base of each transistor is equivalent of the diode's cathode and emitter/collector are equivalent of an anode of the diode.

### **Contact information**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Boris Benenson whose telephone number is (571) 272-2048. The examiner can normally be reached on M-F (8:20-6:00) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2058 or (571) 272-2836. The fax phone



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number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Boris Benenson  
Examiner  
Art Unit 2836

B.B.

1/29/2004



BRIAN SIRCUS  
SUPERVISORY PATENT EXAMINER  
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